FIG.1
PRIOR ART

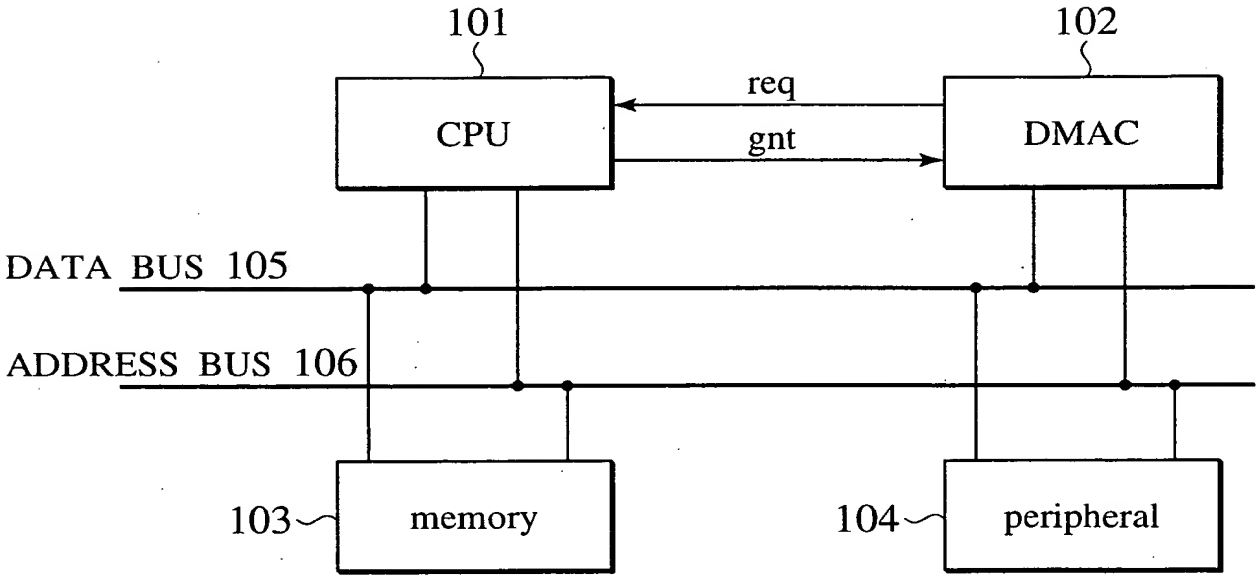


FIG.2
PRIOR ART

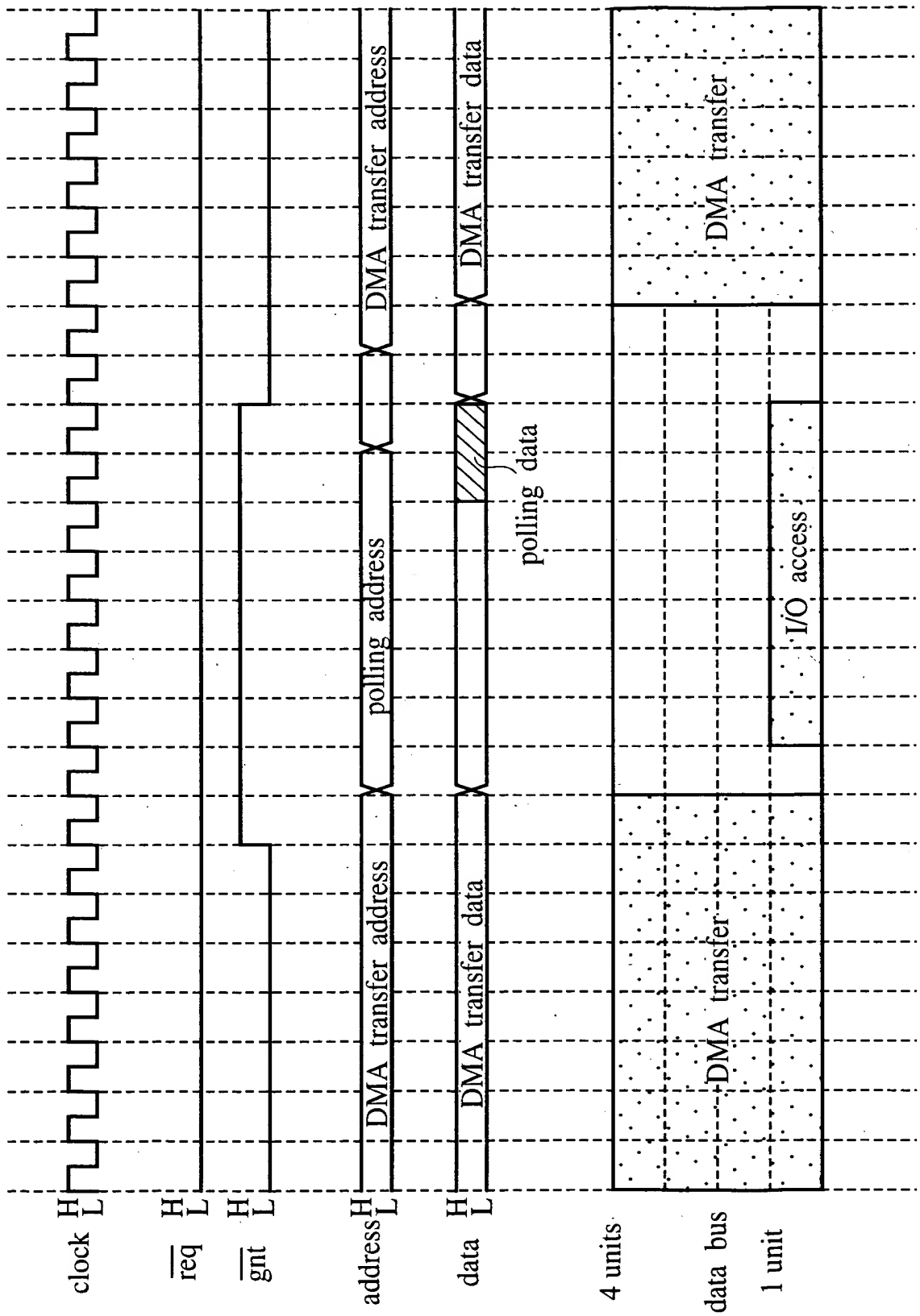


FIG.3
PRIOR ART

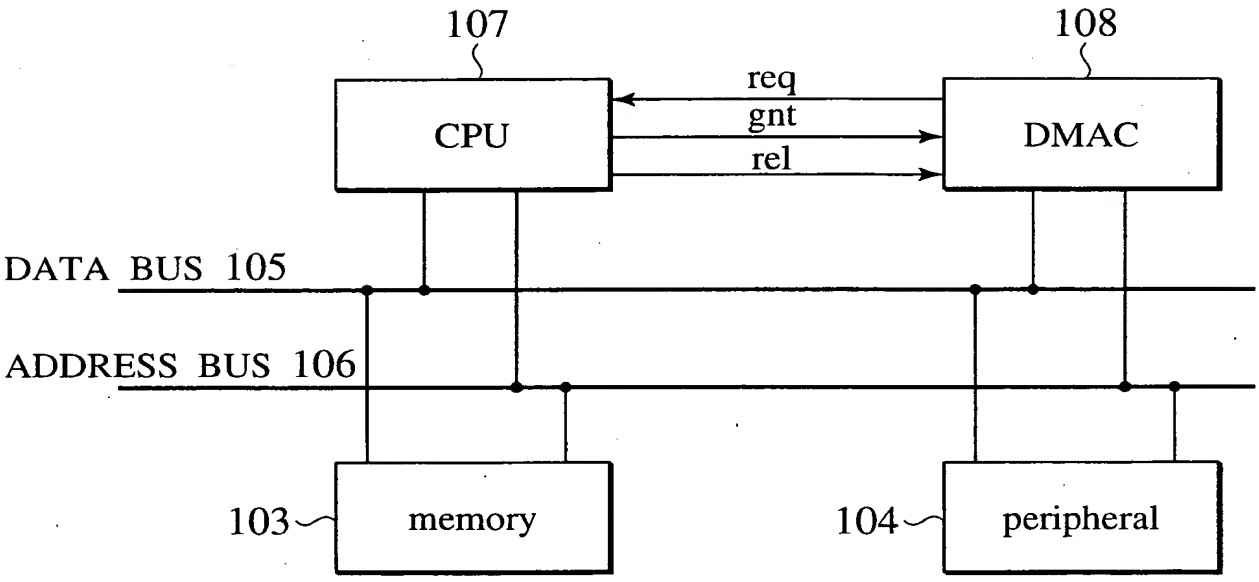


FIG.4
PRIOR ART

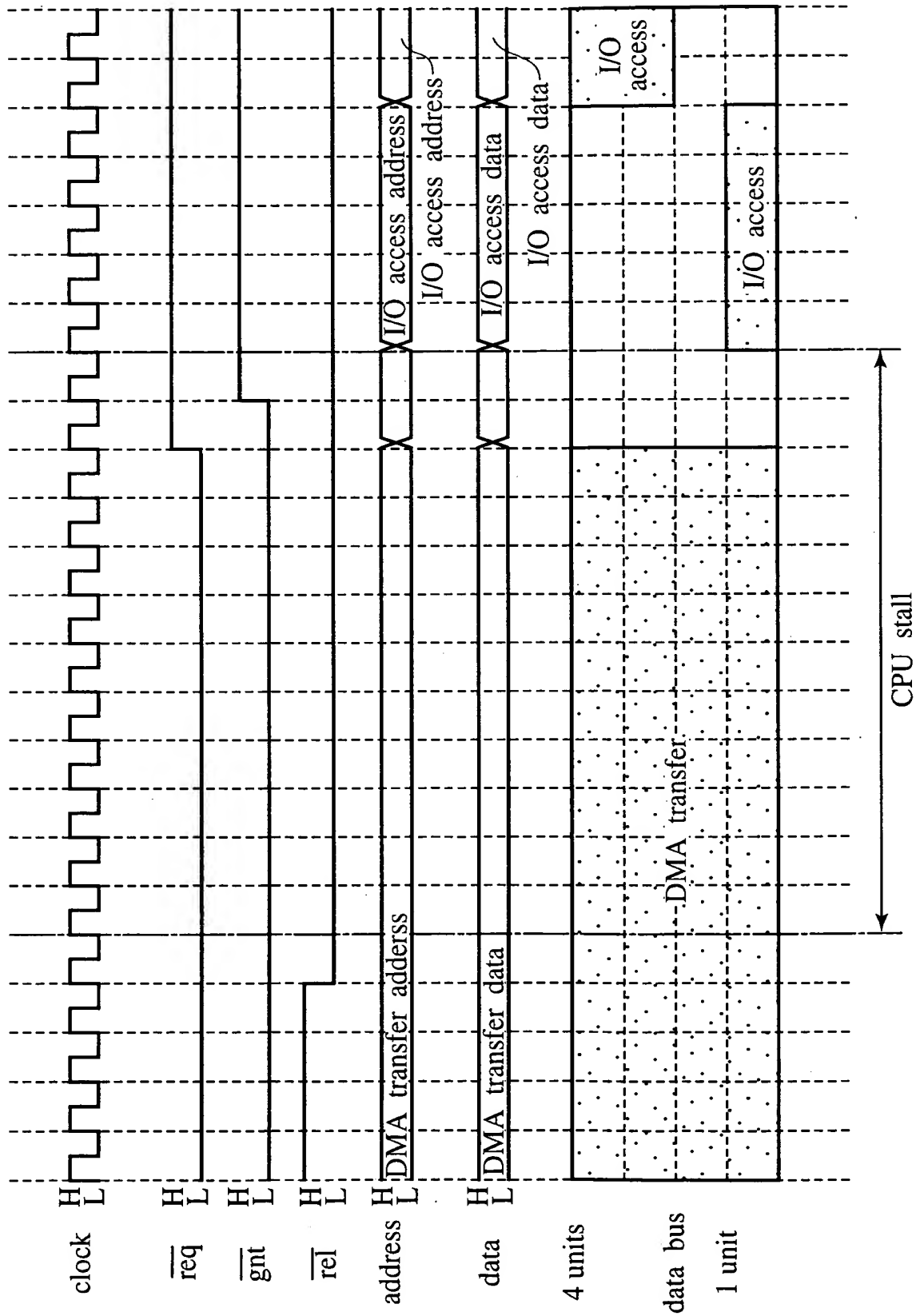


FIG.5

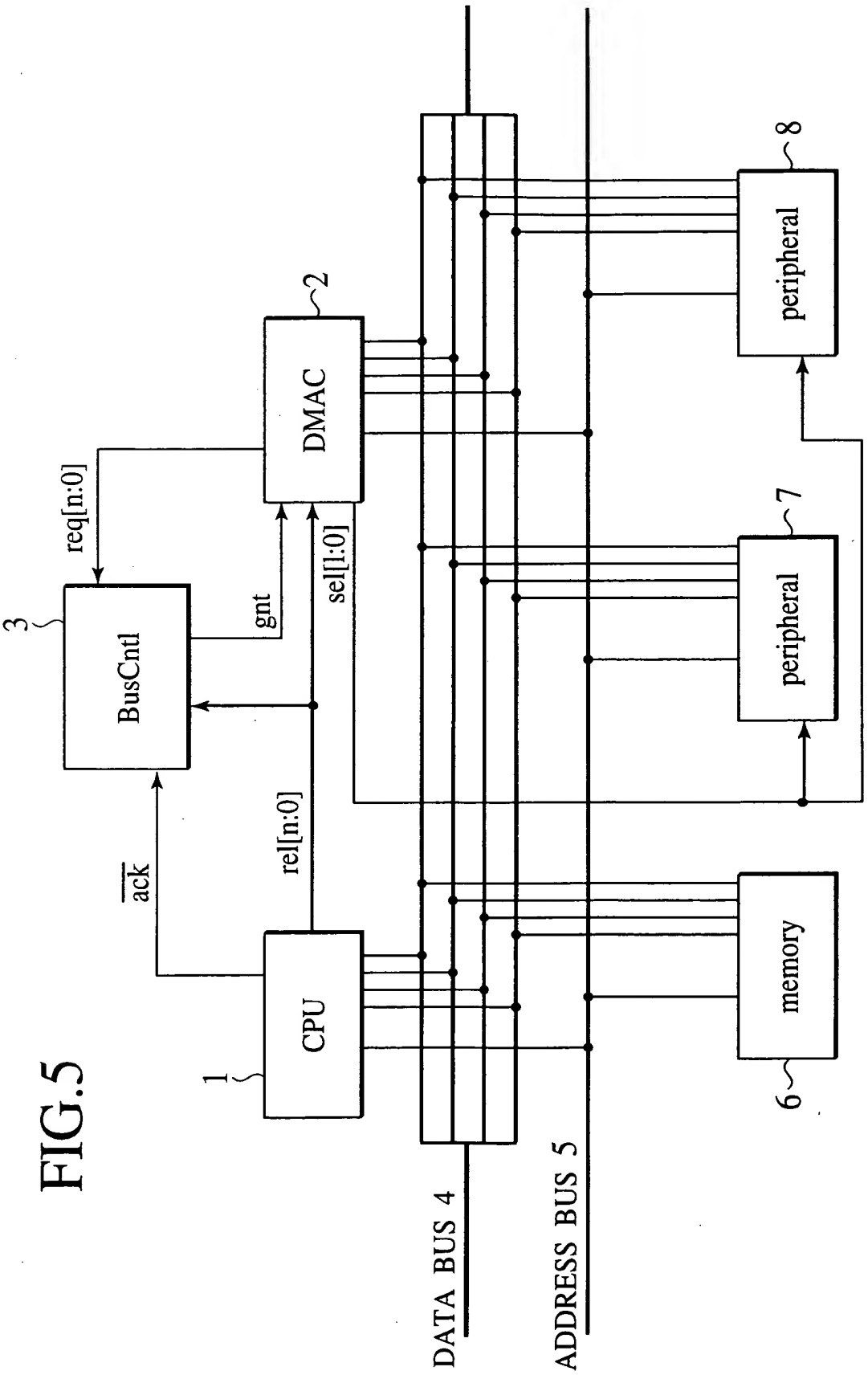
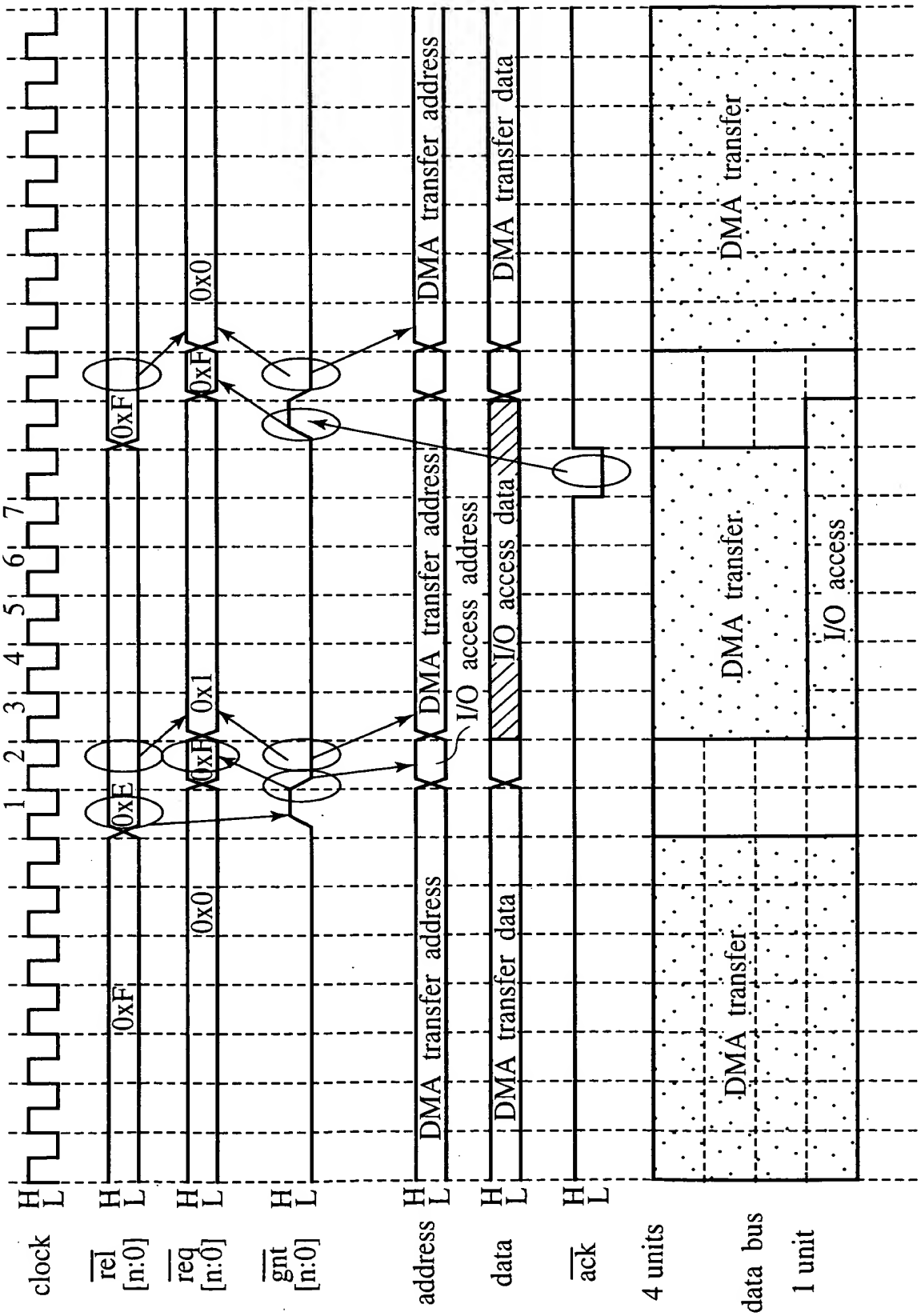


FIG.6


clock
H
L
rel [n:0]
req [n:0]
gnt [n:0]
address
data
ack
4 units
data bus
1 unit
1
2
3
4
5
6
7
0xF
0xE
0xF
0x1
0xF
0x0
0x0
DMA transfer address
DMA transfer data
I/O access address
I/O access data
DMA transfer
I/O access

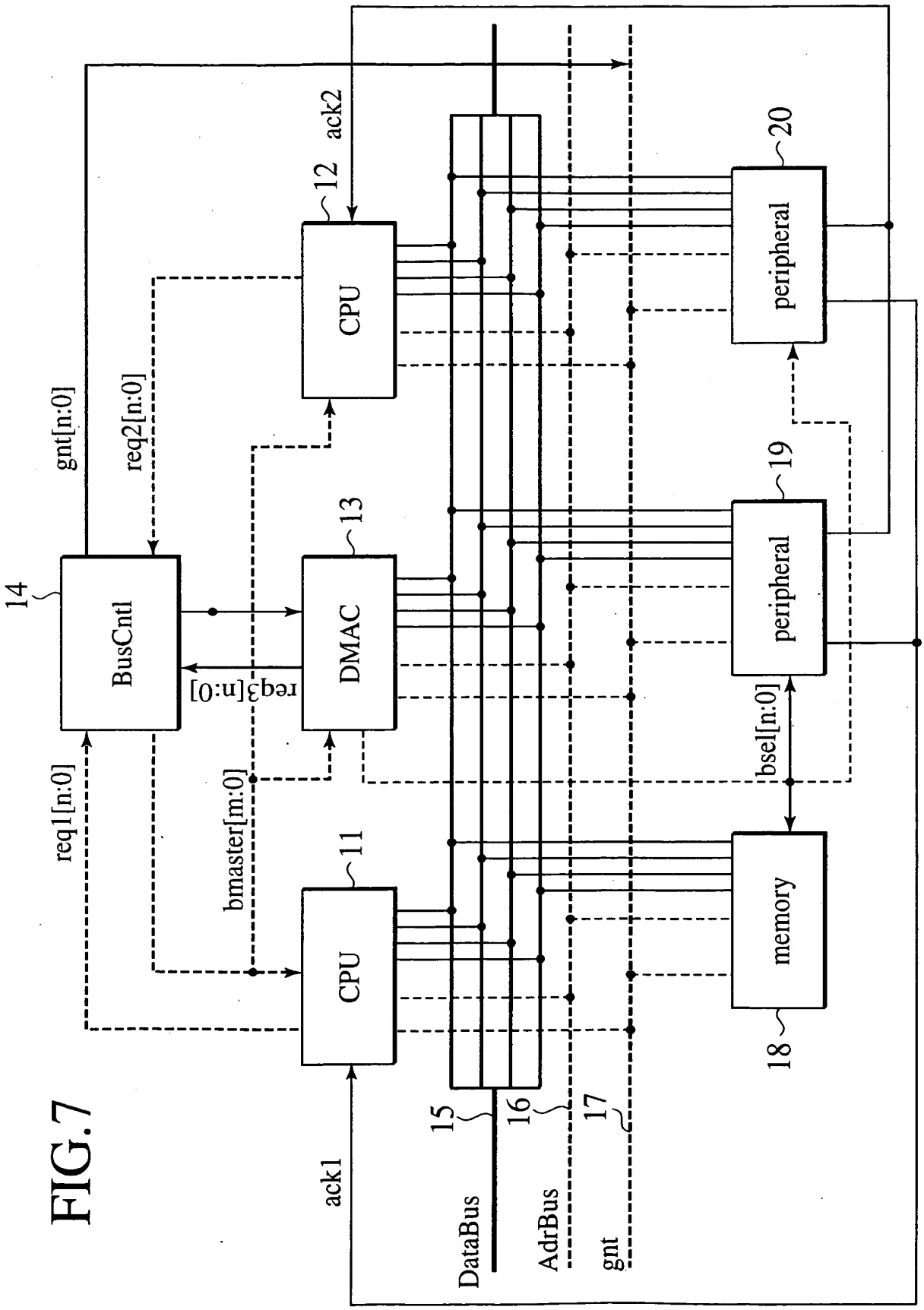
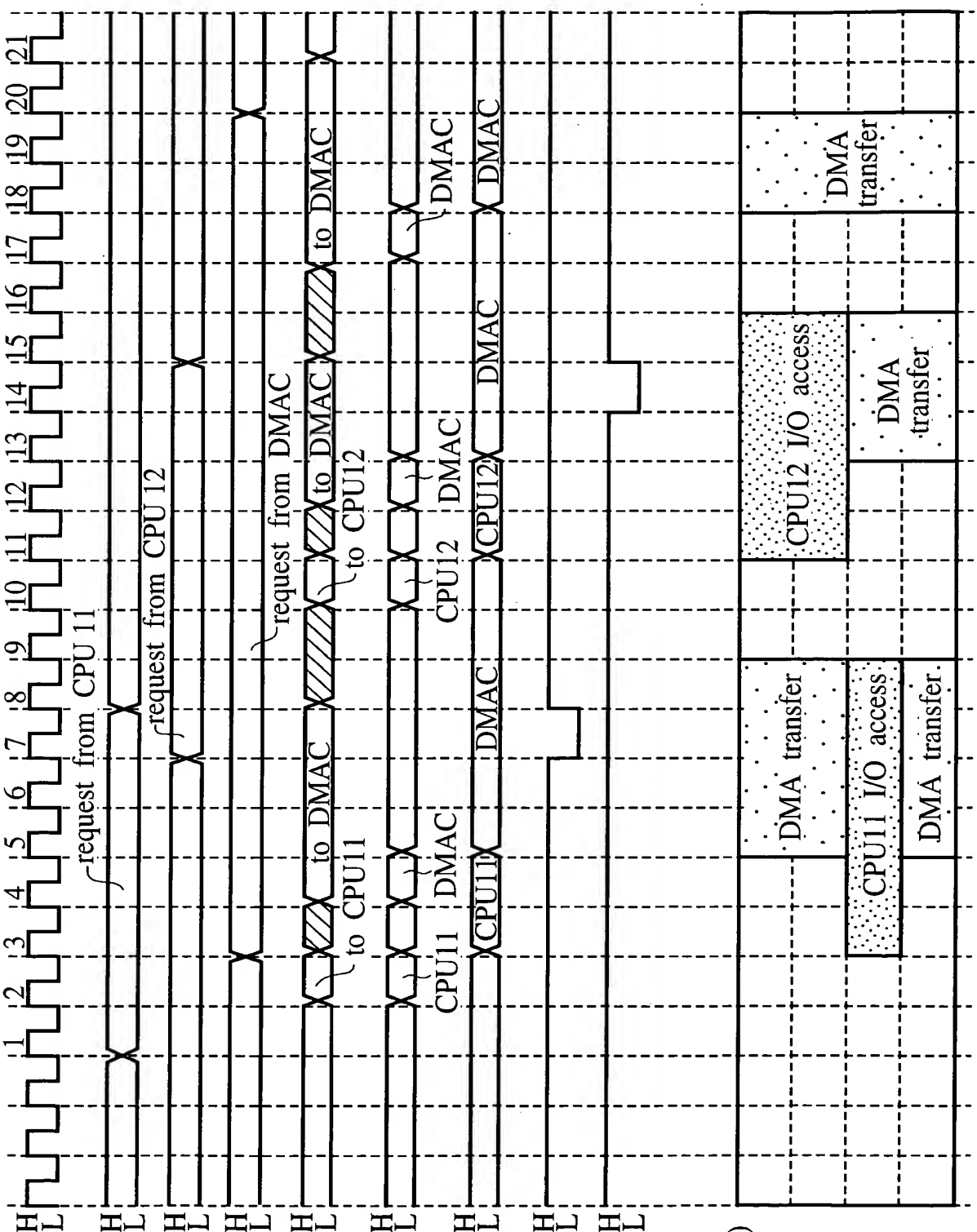


FIG.7

FIG.8


clock
req1[n:0]
req2[n:0]
req3[n:0]
gnt[n:0]
bmaster[m:0]
address
ack1
ack2
(n unit)
data bus
1 unit
0
request from CPU 11
request from CPU 12
request from DMAC
to DMAC
to CPU11
to CPU12
CPU11
CPU12
DMAC
DMA transfer
CPU11 I/O access
CPU12 I/O access

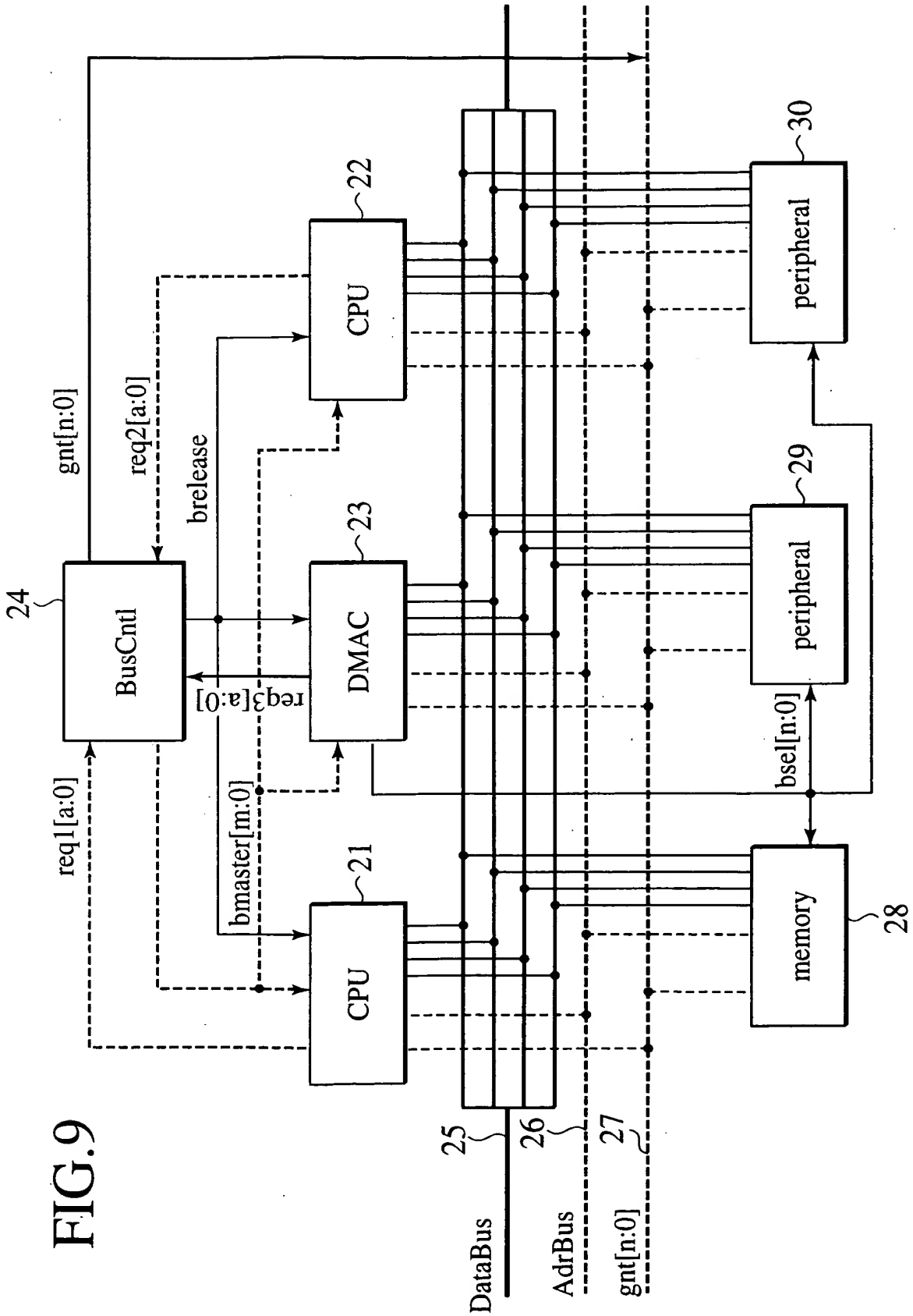
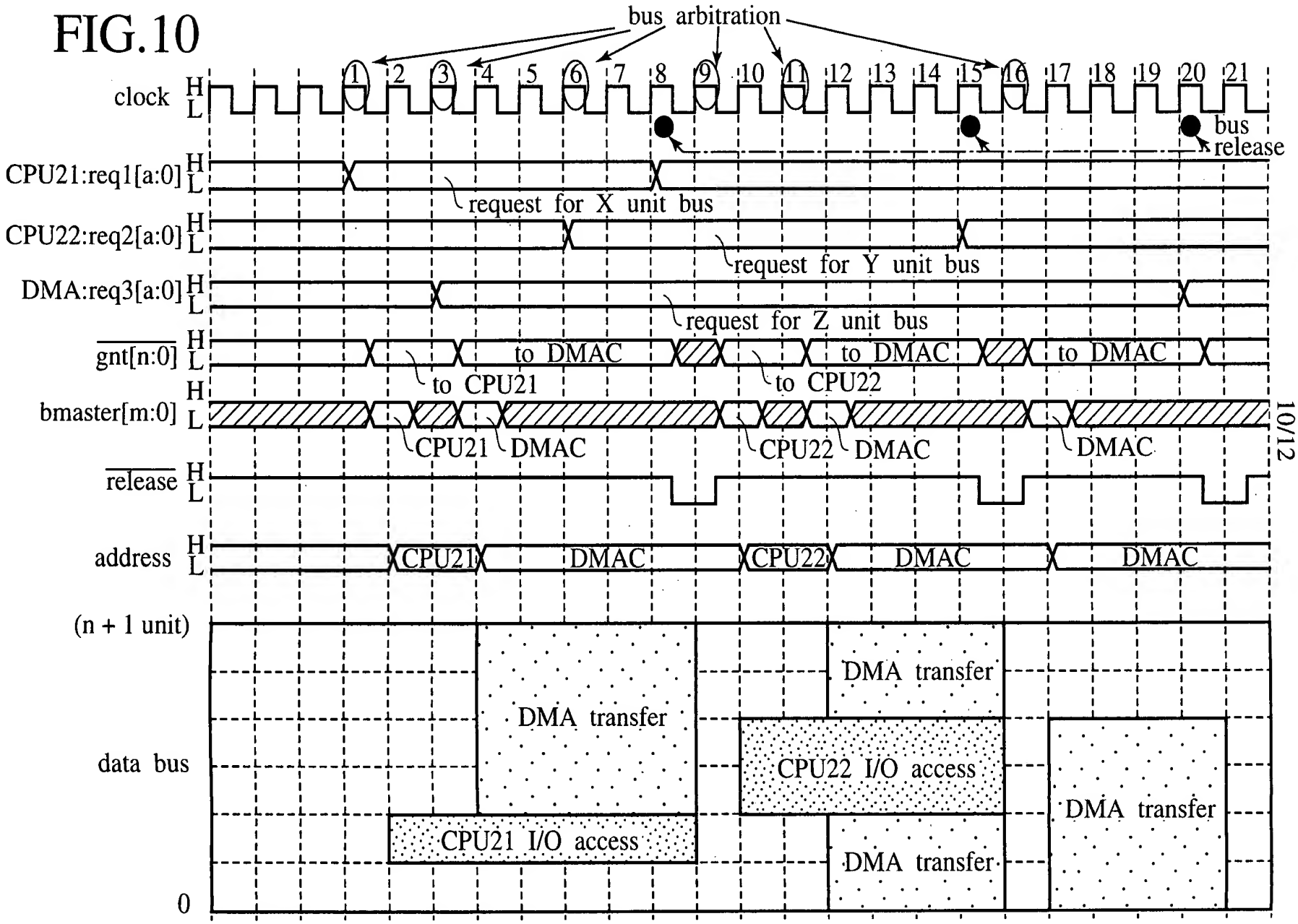

gnt[n:0]
req2[a:0]
brelease
req3[a:0]
bmaster[m:0]
req1[a:0]
BusCntl
24
CPU
22
DMAC
23
CPU
21
peripheral
30
peripheral
29
memory
28
bsel[n:0]
25
26
27
DataBus
AdrBus
gnt[n:0]

FIG.9

FIG.10



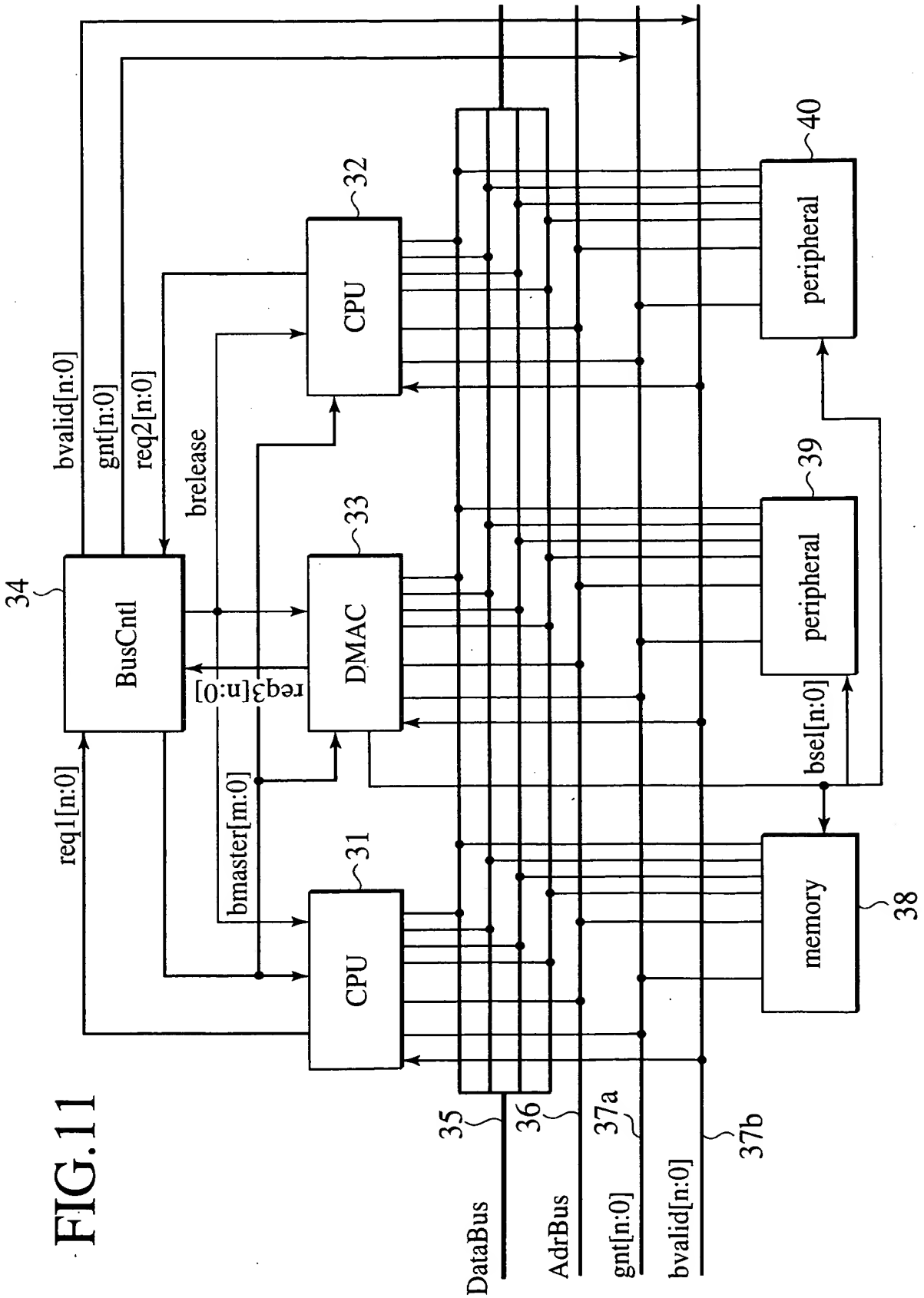
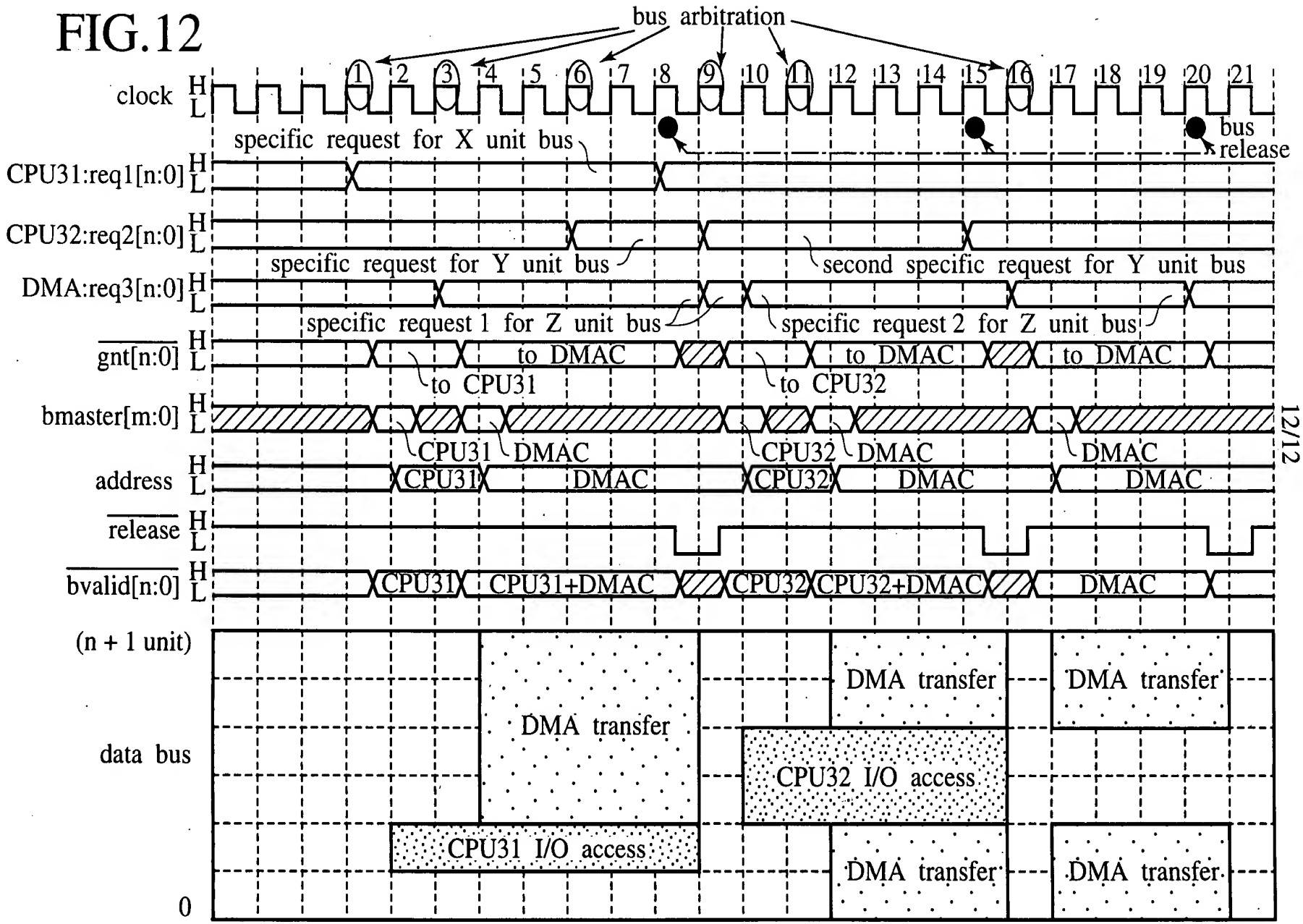

bvalid[n:0]
gnt[n:0]
req2[n:0]
brelease
req3[n:0]
bmaster[m:0]
req1[n:0]
34
BusCntl
CPU
32
DMAC
33
CPU
31
peripheral
40
peripheral
39
bsel[n:0]
memory
38
35
36
37a
37b
DataBus
AdrBus
gnt[n:0]
bvalid[n:0]

FIG.11

FIG.12



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